CLAIMS

I claim:

1. (Original) A method for manufacturing a semiconductor device comprising:

forming an oxide layer on a first surface of an epitaxial layer having damage layer located at a predetermined depth from the first surface, the damaged layer being in parallel alignment with the first surface;

using the oxide layer as a masked, etch the epitaxial layer to create a plurality of pillars, the plurality of pillars being enclosed in a first area of the top surface of the epitaxial layer, the first area having a predefine perimeter, the plurality of pillars being separated from each other by inner trenches and from the perimeter by a perimeter trench, the inner trenches and perimeter trench extend from the first surface to at least the predetermined depth of damaged layer;

forming an oxide layer that coats the pillars, fills the perimeter trench and coats the sides and bottoms of the inner trenches;

removing the oxide layer from at least the sidewalls and bottom of the inner trenches;

performing an etch step with an etchant that etches preferentially the damaged layer; and

forming an layer of silicon dioxide to replace the damaged layer.

2.(Original) The method of claim 1 further comprising the steps of removing the layer of silicon dioxide by an etch step and regrowing a thicker layer of silicon dioxide.

3.(Original) The method of claim 1 further comprising the step of filling the inner trenches with a conductor such as poly silicon.

4.(Original) The method according to claim 1 further comprising the step of filling the inner trenches with an insulator.

5. (Original) The method according to claim 4 wherein the step of filling the inner trenches with an insulator comprises the step of filling the inner trenches with an insulator selected from a group that includes silicon dioxide, silicon nitrite, or a combination of silicon dioxide and silicon nitrite.

6. (Original) The method according to claim 5 wherein the semiconductor device includes a power IC and the method further includes the step of manufacturing a power switch on at least one pillar.

7.(Original) The method according to claim 5 wherein the semiconductor device includes a power IC and the method further includes the step of manufacturing a logic circuit on at least one pillar.

8. (Original) The method according to claim 5 wherein the semiconductor device includes a high frequency analog device and the method further includes the step of manufacturing a high frequency circuit on at least one pillar.

9. (Original) The method according to claim 5 wherein the semiconductor device includes a high speed digital device and the method further includes the step of manufacturing a high speed logic circuit on at least one pillar.

10.(Original) The method according to claim 1 further including the steps of creating a damaged layer at the predetermined depth of the epitaxial layer.

11. (Original) The method according to claim 10 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer;

masking and etching the oxide layer to define at least the first area; and

implanting ions at size and an energy sufficient to damage a region of the semiconductor layer beneath the oxide layer, that coincides with the first area.

12.(Original) The method according to claim 11 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer;

masking and etching the oxide layer to define at least the first area;

implanting N type ions into the semiconductor layer beneath the oxide layer; and

diffusing the implanted ions to form a damaged layer comprising a heavily doped N type region.

13. (Original) The method according to claim 11 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer, the semiconductor layer having a pre-deposition of ions;

masking and etching the oxide layer to define at least the first area;

thermal pre-positioning a high concentration of dopant atoms in at least the first area; and

diffusing the pre-positioned dopant atoms to form a damaged layer comprising a heavily doped N type region.

14.(Original) A method for manufacturing a semiconductor device comprising:

forming an oxide layer on a first surface of an epitaxial layer having damage layer located at a predetermined depth from the first surface, the damaged layer being in parallel alignment with the first surface;

using the oxide layer as a masked, etch the epitaxial layer to create a plurality of pillars, the plurality of pillars being enclosed in a first area of the top surface of the epitaxial layer, the first area having a predefine perimeter, the plurality of pillars being separated from each other by inner trenches and from the perimeter by a perimeter trench, the inner trenches and perimeter trench extend from the first surface to beyond the predetermined depth of damaged layer;

forming an oxide layer that coats the pillars, fills the perimeter trench and coats the sides and bottoms of the inner trenches;

removing the oxide layer from at least the sidewalls and bottom of the inner trenches;

forming a galvanic cell at the damaged layer;

using an HF base etch convert the damaged layer to a layer of porous silicon;

oxidizing the layer of porous silicon;

removing the layer of oxidized porous silicon; and

growing an layer of silicon dioxide to replace the layer of oxidized porous silicon.

15. (Original) The method of claim 14 further comprising the steps of removing the layer of silicon dioxide by an etch step and regrowing a thicker layer of silicon dioxide.

16.(Original) The method of claim 14 further comprising the step of filling the inner trenches with a conductor such as poly silicon.

17. (Original) The method according to claim 14 further comprising the step of filling the inner trenches with an insulator.

18.(Original) The method according to claim 17 wherein the step of filling the inner trenches with an insulator comprises the step of filling the inner trenches with an insulator selected from a group that includes silicon dioxide, silicon nitrite, or a combination of silicon dioxide and silicon nitrite.

19.(Original) The method according to claim 18 wherein the semiconductor device includes a power IC and the method further includes the step of manufacturing a power switch on at least one pillar.

20. (Original) The method according to claim 18 wherein the semiconductor device includes a power IC and the method further includes the step of manufacturing a logic circuit on at least one pillar.

21.(Original) The method according to claim 18 wherein the semiconductor device includes a high frequency analog device and the method further includes the step of manufacturing a high frequency circuit on at least one pillar.

22. (Original) The method according to claim 18 wherein the semiconductor device includes a high speed digital device and the method further includes the step of manufacturing a high speed logic circuit on at least one pillar.

23. (Original) The method according to claim 14 further including the steps of creating a damaged layer at the predetermined depth of the epitaxial layer.

24. (Original) The method according to claim 23 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer;

masking and etching the oxide layer to define at least the first area; and

implanting ions at size and an energy sufficient to damage a region of the semiconductor layer beneath the oxide layer, that coincides with the first area.

25.(Original) The method according to claim 23 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer;

masking and etching the oxide layer to define at least the first area;

implanting N type ions into the semiconductor layer beneath the oxide layer; and

diffusing the implanted ions to form a damaged layer comprising a helvella doped N type region.

26. (Original) The method according to claim 23 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer, the semiconductor layer having a pre-deposition of ions;

masking and etching the oxide layer to define at least the first area;

thermal pre-positioning a high concentration of dopant atoms in at least the first area; and

diffusing the pre-positioned dopant atoms to form a damaged layer comprising a heavily doped N type region.

27.(Original) A method for manufacturing a semiconductor device comprising:

forming an oxide layer on a first surface of an epitaxial layer having damage layer located at a predetermined depth from the first surface, the damaged layer being in parallel alignment with the first surface;

using the oxide layer as a masked, etch the epitaxial layer to create a pillar, the pillar being enclosed in a first area of the top surface of the epitaxial layer, the first area having a predefine perimeter, the pillar being separated from the perimeter by a perimeter trench, on at least a first side by inner trenches on the remaining sides, the trenches extend from the first surface to beyond the predetermined depth of damaged layer;

forming an oxide layer that coats the pillar, fills the perimeter trench, and coats the sides and bottoms of the inner trenches;

removing the oxide layer from at least the sidewalls and bottom of the inner trenches;

performing an etch step with an etchant that etches preferentially the damaged layer; and

growing an layer of silicon dioxide to replace the damaged layer.

28.(Original) The method of claim 27 further comprising the steps of removing the layer of silicon dioxide by an etch step and regrowing a thicker layer of silicon dioxide.

29.(Original) The method of claim 27 further comprising the step of filling the inner trenches with a conductor such as poly silicon.

30.(Original) The method according to claim 27 further comprising the step of filling the inner trenches with an insulator.

31. (Original) The method according to claim 30 wherein the step of filling the inner trenches with an insulator comprises the step of filling the inner trenches with an insulator selected from a group that includes silicon dioxide, silicon nitrite, or a combination of silicon dioxide and silicon nitrite.

32. (Original) The method according to claim 31 wherein the semiconductor device includes a power IC and the method further includes the step of manufacturing a power switch on at least one pillar.

33.(Original) The method according to claim 31 wherein the semiconductor device includes a power IC and the method further includes the step of manufacturing a logic circuit on at least one pillar.

34.(Original) The method according to claim 31 wherein the semiconductor device includes a high frequency analog device and the method further includes the step of manufacturing a high frequency circuit on at least one pillar.

35. (Original) The method according to claim 31 wherein the semiconductor device includes a high speed digital device and the method further includes the step of manufacturing a high speed logic circuit on at least one pillar.

36. (Original) The method according to claim 27 further including the steps of creating a damaged layer at the predetermined depth of the epitaxial layer.

37. (Original) The method according to claim 36 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer;

masking and etching the oxide layer to define at least the first area; and

implanting ions at size and an energy sufficient to damage a region of the semiconductor layer beneath the oxide layer, that coincides with the first area.

38. (Original) The method according to claim 36 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer;

masking and etching the oxide layer to define at least the first area;

implanting N type ions into the semiconductor layer beneath the oxide layer; and

diffusing the implanted ions to form a damaged layer comprising a heavily doped N type region.

39. (Original) The method according to claim 36 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer, the semiconductor layer having a pre-deposition of ions;

masking and etching the oxide layer to define at least the first area;

thermal pre-positioning a high concentration of dopant atoms in at least the first area; and

diffusing the pre-positioned dopant atoms to form a damaged layer comprising a heavily doped N type region.

40. (Original) A method for manufacturing a semiconductor device comprising:

forming an oxide layer on a first surface of an epitaxial layer having damage layer located at a predetermined depth from the first surface, the damaged layer being in parallel alignment with the first surface;

using the oxide layer as a masked, etch the epitaxial layer to create a pillar, the pillar being enclosed in a first area of the top surface of the epitaxial layer, the first area having a predefined perimeter, the pillar being separated from the perimeter by a perimeter trench along a first side, and with internal trenches on the second side, the inner trenches and perimeter trench extend from the first surface to beyond the predetermined depth of damaged layer;

forming an oxide layer that coats the pillar, fills the perimeter trench, and coats the sides and bottoms of the inner trenches;

removing the oxide layer from at least the sidewalls and bottom of the inner trenches;

forming a galvanic cell at the damaged layer;

using an HF base etch convert the damaged layer to a layer of porous silicon;

oxidizing the layer of porous silicon;

removing the layer of oxidized porous silicon; and

growing an layer of silicon dioxide to replace the layer of oxidized porous silicon.

41. (Original) The method of claim 40 further comprising the steps of removing the layer of silicon dioxide by an etch step and regrowing a thicker layer of silicon dioxide.

42. (Original) The method of claim 40 further comprising the step of filling the inner trenches with a conductor such as poly silicon.

43. (Original) The method according to claim 40 further comprising the step of filling the inner trenches with an insulator.

44. (Original) The method according to claim 43 wherein the step of filling the inner trenches with an insulator comprises the step of filling the inner trenches with an insulator selected from a group that includes silicon dioxide, silicon nitrite, or a combination of silicon dioxide and silicon nitrite.

45. (Original) The method according to claim 44 wherein the semiconductor device includes a power IC and the method further includes the step of manufacturing a power switch on at least one pillar.

46. (Original) The method according to claim 44 wherein the semiconductor device includes a power IC and the method further includes the step of manufacturing a logic circuit on at least one pillar.

47. (Original) The method according to claim 44 wherein the semiconductor device includes a high frequency analog device and the method further includes the step of manufacturing a high frequency circuit on at least one pillar.

48. (Original) The method according to claim 44 wherein the semiconductor device includes a high speed digital device and the method further includes the step of manufacturing a high speed logic circuit on at least one pillar.

49. (Original) The method according to claim 40 further including the steps of creating a damaged layer at the predetermined depth of the epitaxial layer.

50. (Original) The method according to claim 49 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer;

masking and etching the oxide layer to define at least the first area; and

implanting ions at size and an energy sufficient to damage an area of the semiconductor layer beneath the oxide layer, that coincides with the first area.

51. (Original) The method according to claim 49 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer;

masking and etching the oxide layer to define at least the first area;

implanting N type ions into the semiconductor layer beneath the oxide layer; and

diffusing the implanted ions to form a damaged layer comprising a heavily doped N type region.

52. (Original) The method according to claim 49 wherein the steps of creating a damaged layer at the predetermined depth of the epitaxial layer comprises;

growing an oxide layer on the surface of a semiconductor layer such as a starting wafer, the semiconductor layer having a pre-deposition of ions;

masking and etching the oxide layer to define at least the first area;

thermal pre-positioning a high concentration of dopant atoms in at least the first area; and

diffusing the implanted ions to form a damaged layer comprising a heavily doped N type region.